CLAIMS

The invention claimed is:

1. A non-volatile device comprising:

a crystalline layer separated from a substrate by a first insulative material; the crystalline layer being less than or equal to about 2000 Å thick and comprising a material which includes silicon and germanium;

a floating charge trapping media over the crystalline layer;

a pair of source/drain regions proximate the charge trapping media and extending into the crystalline layer such that at least a portion of the source/drain regions are within the crystalline layer; the portion of the source/drain regions within the crystalline layer being contained within a single crystal of the material which includes silicon and germanium;

a second insulative material over the charge trapping media; and

a control gate over the second insulative material.

2. The device of claim 1 wherein the charge trapping media is a floating gate comprising conductively doped silicon.

3. The device of claim 2 wherein the second insulative material comprises ONO.

4. The device of claim 1 wherein the charge trapping media is a floating plate.

5. The device of claim 4 wherein the second insulative material comprises ONO.

6. The device of claim 4 wherein the second insulative material comprises a high k dielectric material.

7. The device of claim 4 wherein the floating plate comprises silicon enriched oxide.

8. The device of claim 4 wherein the floating plate comprises silicon enriched nitride.

9. The device of claim 1 wherein the material which includes silicon and germanium comprises from about 10 to about 60 atomic percent germanium.

10. The device of claim 1 wherein the crystalline layer is polycrystalline.

11. The device of claim 1 wherein the crystalline layer is monocrystalline.

12. The device of claim 1 wherein the crystalline layer has a relaxed crystalline lattice, and further comprising a strained crystalline lattice layer between the relaxed crystalline lattice and the charge-trapping media.

13. The device of claim 12 wherein the strained crystalline lattice includes silicon.

14. The device of claim 12 wherein the strained crystalline lattice includes silicon and germanium.

15. The device of claim 1 wherein the source/drain regions are n-type regions.

16. The device of claim 1 wherein the substrate comprises a semiconductive material.

17. The device of claim 1 wherein the substrate comprises glass.

18. The device of claim 1 wherein the substrate comprises aluminum oxide.

19. The device of claim 1 wherein the substrate comprises silicon dioxide.

20. The device of claim 1 wherein the substrate comprises a metal.

21. The device of claim 1 wherein the substrate comprises a plastic.

22. A memory device comprising the non-volatile device of claim 1.

23. A logic device comprising the non-volatile device of claim 1.

24. A non-volatile device construction, comprising:

a first electrically insulative material;

a first crystalline Si/Ge layer over the first electrically insulative material; the first crystalline Si/Ge layer having a relaxed crystalline lattice;

a second crystalline Si/Ge layer over the first crystalline Si/Ge layer; the second crystalline Si/Ge layer having a strained crystalline lattice;

an electrically floating element over the second crystalline Si/Ge layer;

an active region extending into the first and second crystalline Si/Ge layers proximate the floating element, the active region including a pair of source/drain regions gatedly connected with one another by the floating element; the active region within the first crystalline Si/Ge layer being within a single crystal of the first crystalline Si/Ge layer; and

a control gate proximate the floating element and spaced from the floating element by one or more second insulative materials.

25. The construction of claim 24 wherein the floating element is a floating gate.

26. The construction of claim 25 wherein the floating gate comprises conductively-doped silicon and wherein the one or more second insulative materials comprise ONO.

27. The construction of claim 24 wherein the floating element is a floating plate.

28. The construction of claim 27 wherein the one or more second insulative materials comprise ONO.

29. The construction of claim 27 wherein the one or more second insulative materials comprise a high k dielectric material.

30. The construction of claim 27 wherein the floating plate comprises silicon enriched oxide.

31. The construction of claim 27 wherein the floating plate comprises silicon enriched nitride.

32. The construction of claim 24 wherein the first electrically insulative material is supported by a substrate; and wherein the crystalline layer and first electrically insulative material are together comprised by an SOI construction.

33. The construction of claim 32 wherein the substrate comprises a semiconductive material.

34. The construction of claim 32 wherein the substrate comprises glass.

35. The construction of claim 32 wherein the substrate comprises aluminum oxide.

36. The construction of claim 32 wherein the substrate comprises silicon dioxide.

37. The construction of claim 32 wherein the substrate comprises a metal.

38. The construction of claim 32 wherein the substrate comprises a plastic.

39. An electronic system comprising the construction of claim 32.

40. The electronic system of claim 39 wherein the non-volatile device is comprised by an EPROM, EEPROM, flash or NVRAM.

41. The electronic system of claim 39 wherein the non-volatile device is comprised by a programmable gate array.

42. An electronic system, the electronic system comprising a memory device, the memory device including:

an array of memory cells, at least some of the memory cells including an electrically floating element and a control gate separated from the floating element by one or more insulative materials; the at least some of the memory cells further comprising active regions proximate the floating elements; the active regions including source/drain regions gatedly connected by the floating elements; the active regions extending into a crystalline Si/Ge layer;

addressing circuitry coupled to the array of memory cells for accessing individual memory cells in the array of memory cells; and

a read circuit coupled to the memory cell array for reading data from memory cells in the array of memory cells.

43. The electronic system of claim 42 wherein the floating elements are floating gates.

44. The electronic system of claim 42 wherein the floating elements are floating plates.

45. The electronic system of claim 42 wherein the active regions within the crystalline layer are each individually entirely contained within a single crystal of the crystalline layer.

46. The electronic system of claim 45 wherein the crystalline layer is polycrystalline.

47. The electronic system of claim 45 wherein the crystalline layer is monocrystalline.

48. The electronic system of claim 42 wherein the crystalline layer has a relaxed crystalline lattice, and further comprising a strained crystalline lattice layer between the relaxed crystalline lattice and the floating elements.

49. The electronic system of claim 48 wherein the strained crystalline lattice includes silicon.

50. The electronic system of claim 48 wherein the strained crystalline lattice includes silicon and germanium.